Product Datasheet

MK8000

Highly integrated UWB SoC compliant to IEEE802.15.4/15.4z and FiRa Standard

November 26, 2024
V0.95

Revision History

Revision	Date	Description	Author
V0.1	Dec23, 2019	Initial version	
V0.2	May 8, 2020	Updated	
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V0.94	April 28, 2023	Updated parameters for LGA	
V0.95	Nov 26, 2024	Updated more parameters in chapter5	

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1. Overview of MK8000

MK8000 is a UWB (Ultra-Wideband) technology based highly integrated WSoC (Wireless SoC) compliant to IEEE802.15.4/15.4z and FiRa standards with high precision 3-D location capability. It integrates ARM® Cortex M0 processor with various memory options and power states optimized for mobile and IoT applications. Dedicated AES engine and TRNG generator ensures secure ranging and data communication.

2. Key features

- Basic features
  - IEEE802.15.4, IEEE802.15.4z and FiRa UWB standard compliant
  - Supports UWB band 1 and 2 (3.1GHz ~ 9 GHz) for worldwide use.
  - Support CCA/DAA/LDC features.
  - 4 receive channels and 1 transmit channel for Angle of Arrival (AoA) measurement.
  - Compliant with FCC, SRRC, ETSI, ARIB spectrum requirements.
  - Programmable PA output in 0.5dB step with maximum output 10 dBm
  - -93.5dBm RX sensitivity for 6.8Mbps data rate @CH9
  - Supports 110 Kbps, 850 Kbps, 6.8 Mbps, 27.2 Mbps, and 54 Mbps data communication.
  - Supports all BPRF and HPRF modes
  - Integrated TRX switch and matching network.
  - High precision 3-D location capability, 10cm ranging and 5° angle measurement accuracy
  - Supports payload size up to 1023 bytes
- Power supply and consumption
  - Supply voltage 1.8V~3.6V
  - Integrated DC-DC (buck) and LDO
  - < 6.0 µA deep power down current
  - < 4 µs MCU wakeup time from deep power down mode
  - < 120 µs TRX fast wakeup time
  - Less than 43mA RX and TX peak current
- Security
  - Fully integrated AES128 security engine
  - Integrated TRNG
- Compact 5x5 LGA40 package
- Temperature
  - -40°C - 85°C
- Microcontroller
  - Integrated 32-bit ARM Cortex-M0 MCU running up to 62.4MHz
  - 512KB Flash and 192kB RAM
  - Integrated 8-channel DMA

- Peripherals
  - Up to 18 GPIO pins, and all GPIOs can be configured as interrupt pin.
  - Integrated UART/SPI/I2C interface.
  - Integrated 38.4-MHz crystal oscillator, can also take 38.4-MHz clock input
  - Low power 32KHz and 48MHz RC oscillator
  - 32.768-kHz crystal oscillator
  - LED drive directly, 10mA/IO, support 4 LED working at the same time.
  - 4 general purpose 16-bit/32-bit timers, and PWM output support
  - Fully integrated programmable BOD/BOR
  - Integrated battery monitor and temperature sensor
- Low BOM-cost
  - Less than 10 external components

3. Pin Diagram

3.1 LGA Package

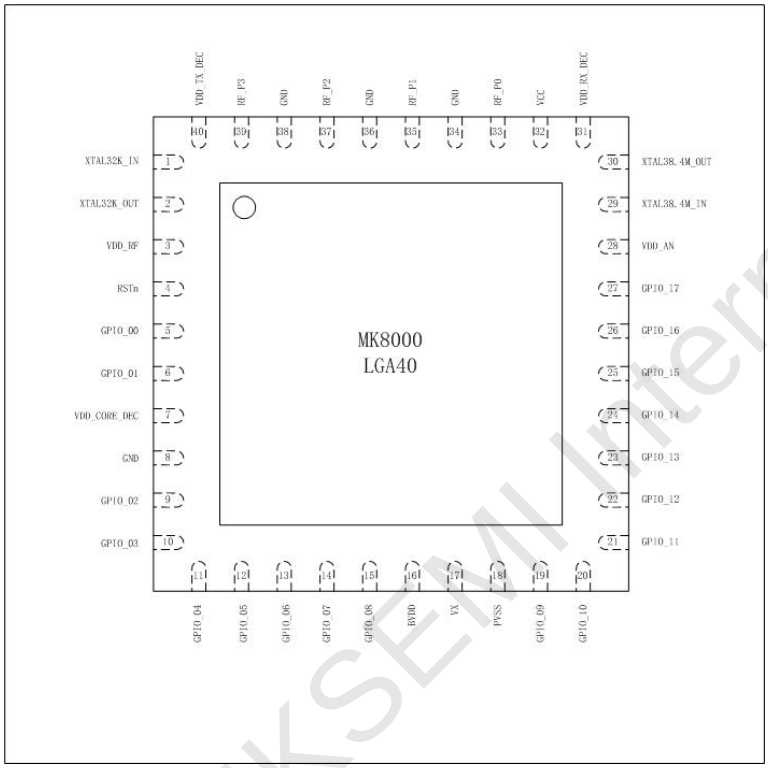


Figure 1 LGA40 package pin diagram

3.2 Pin Description

Table 1 Pin Description

Signal Name		Rest State	Type	Description
1	XTAL32K_IN	-	AI	32.768K crystal oscillator clock input.
2	XTAL32k_OUT	-	AO	32.768K crystal oscillator output.
3	VDD_RF	AI	-	RF power supply
4	RSTn	PU	I	Active low reset input
5	GPIO_00	Hi-Z		General purpose input/output pin. Or use as an interrupt pin.

6	GPIO_01	Hi-Z		General purpose input/output pin. Or use as an interrupt pin.
7	VDD_CORE_DEC	AO	-	Core Voltage supply
8	GND	-	-	IC ground
9	GPIO_02	Hi-Z	I/O	*General purpose input/output pin. Or use as an interrupt pin.*
10	GPIO_03	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin. *When this pin is connected to ground during IC bootup, IC will enter ISP mode.*
11	GPIO_04	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
12	GPIO_05	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
13	GPIO_06	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
14	GPIO_07	Hi-Z	I/O	General purpose input/output pin. or use as an interrupt pin.
15	GPIO_08	Hi-Z	I/O	General purpose input/output pin. Or use as an interrupt pin.
16	BVDD	AI	-	Internal DC-DC Power supply input, 1.8~3.6V. When in eFuse programing, the voltage should be higher than 2.5V.
17	VX	AO	-	DC/DC regulator output, should connect to inductor and then a capacitor to ground, leave it open when use external DC/DC
18	PVSS		-	Internal DC-DC converter ground
19	GPIO_09	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
20	GPIO_10	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
21	GPIO_11	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.

22	GPIO_12	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
23	GPIO_13	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
24	GPIO_14	Hi-Z	I/O	General purpose input/output pin, or use as an interrupt pin.
25	GPIO_15	Hi-Z	I/O	General purpose input/output pin, Default function. Or use as an interrupt pin.
26	GPIO_16	Hi-Z	I/O	General purpose input/output pin. Or use as an interrupt pin.
27	GPIO_17	Hi-Z	I/O	General purpose input/output pin or interrupt pin.
28	VDD_AN	AI	-	Analog part power supply
29	XTAL38.4M_IN	-	AI	38.4M crystal oscillator clock input. Or external clock input pin, such as TCXO or 38.4Mhz clock from the system.
30	XTAL38.4M_OUT	-	AO	38.4M crystal oscillator output. If external clock, leave it floating
31	VDD _RX_DEC	AO	-	VDD decoupling for receiver, internal power output.
32	VCC	AI	-	Vcc supply
33	RF_P0	-	RF	RF port 0
34	GND	-	-	Ground
35	RF_P1	-	RF	RF port 1
36	GND	-	-	Ground
37	RF_P2	-	RF	RF port 2, Low Band
38	GND		-	GND
39	RF_P3	-	RF	RF port 3, High band
40	VDD _TX_DEC	AO	-	VDD decoupling for Transmitter, internal power output.

4. Functional Description

4.1 MK8000 Architecture

The MK8000 is a UWB based wireless SoC (WSoC). It integrates a low power ARM® Cortex®-M0 core, an ultra low power UWB subsystem, a highly efficient LSP (Location Signal Processor) co-processor dedicated to ranging and AoA computation, system memories, DMA, PMU, CMU, RMU, analog and digital peripherals, I/Os and security engine. Figure 2 shows the top level SoC architecture.

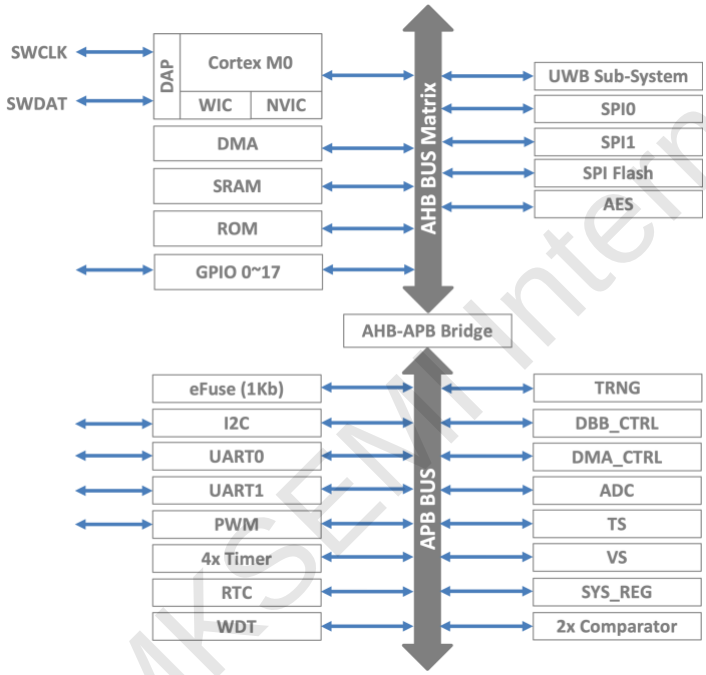


Figure 2 MK8000 WSoC Architecture

4.2 ARM Cortex-M0 processor

The MCU is a 32-bit ARM Cortex-M0 core which offers the following features and benefits:

- Tight integration of system peripherals
- Thumb instruction set combines high code density with 32-bit performance
- Power control optimization of system components
- Integrated sleep modes for low power consumption
- Fast code execution permits slower processor clock or increases sleep mode time
- Hardware multiplier
- SWD reduces the number of pins required for debugging
- Deterministic, high-performance interrupt handling for time-critical application

4.3 LSP Co-processor

MK8000 integrates an LSP (Location Signal Processor) co-processor as a hardware accelerator to offload the MCU from routine computations in ranging, AoA and location algorithms. It integrates real and complex floating point computation engines for vector summation, subtraction, multiplication, inner product, element inverse, etc operations. The LSP is an AHB bus slave with DMA integrated. Once

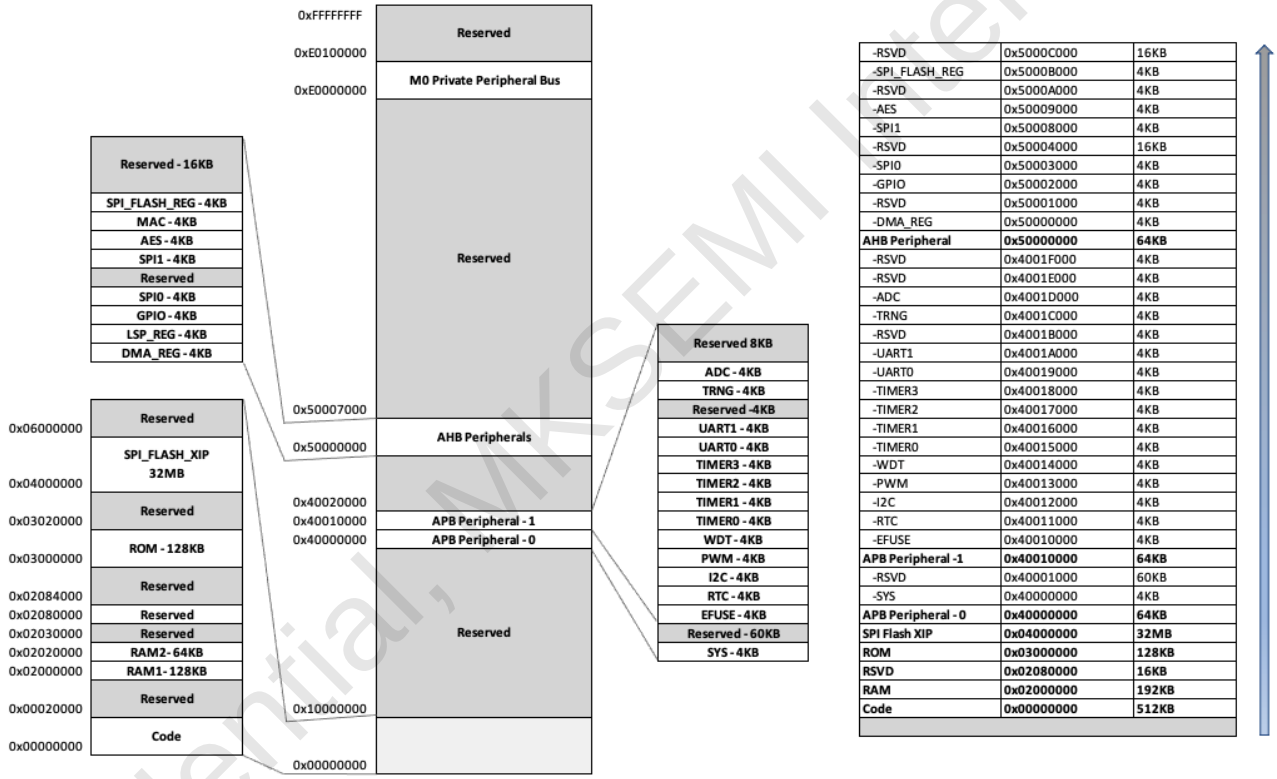
programmed, the LSP will load data and perform the computation automatically. It will generate an interrupt to the MCU once the computation has been accomplished.

4.4 Memory

The MK8000 integrates the following memory units to offer high flexibility in different applications:

- 128KB ROM
- 192KB SRAM
- 1Kb eFuse
- Optionally 512KB NOR Flash

The MCU is 32-bit with an address space of 4GB. It is shared among system memory, ROM, system registers, peripheral registers and general purpose memory. The address space ranges from 0x0000 0000 to 0xFFFF FFFF. Figure 3 shows the detailed memory address map of MK8000 system.



-RSVD	0x5000C000	16KB
-SPI_FLASH_REG	0x5000B000	4KB
-RSVD	0x5000A000	4KB
-AES	0x50009000	4KB
-SPI1	0x50008000	4KB
-RSVD	0x50004000	16KB
-SPI0	0x50003000	4KB
-GPIO	0x50002000	4KB
-RSVD	0x50001000	4KB
-DMA_REG	0x50000000	4KB
AHB Peripheral	**0x50000000**	**64KB**
-RSVD	0x4001F000	4KB
-RSVD	0x4001E000	4KB
-ADC	0x4001D000	4KB
-TRNG	0x4001C000	4KB
-RSVD	0x4001B000	4KB
-UART1	0x4001A000	4KB
-UART0	0x40019000	4KB
-TIMER3	0x40018000	4KB
-TIMER2	0x40017000	4KB
-TIMER1	0x40016000	4KB
-TIMER0	0x40015000	4KB
-WDT	0x40014000	4KB
-PWM	0x40013000	4KB
-I2C	0x40012000	4KB
-RTC	0x40011000	4KB
-EFUSE	0x40010000	4KB
APB Peripheral -1	**0x40010000**	**64KB**
-RSVD	0x40001000	60KB
-SYS	0x40000000	4KB
APB Peripheral - 0	**0x40000000**	**64KB**
SPI Flash XIP	**0x04000000**	**32MB**
ROM	**0x03000000**	**128KB**
RSVD	**0x02080000**	**16KB**
RAM	**0x02000000**	**192KB**
Code	**0x00000000**	**512KB**

Figure 3 Memory address map

4.4.1 ROM

The MK8000 integrates 128KB ROM which stores a bootloader with SPI support and a UWB protocol stack compliant with IEEE802.15.4/15.4z and FiRa standards.

4.4.2 Embedded SRAM

MK8000 integrates 192 kB SRAM with high throughput and individual power control capability for low-power operation. The SRAM is divided into 9 memory blocks, each with separate power control to optimize the power consumption based on the application requirements. Table 2 shows the detailed information of memory banks.

Table 2 SRAM memory banks

SRAM Block	Description	Size (K bytes)	Start Address	End Address
0	RAM1	4	0x0200 0000	0x0200 0FFF
1		4	0x0200 1000	0x0200 1FFF
2		8	0x0200 2000	0x0200 3FFF
3		16	0x0200 4000	0x0200 7FFF
4		32	0x0200 8000	0x0200 FFFF
5		32	0x0201 0000	0x0201 7FFF
6		32	0x0201 8000	0x0201 FFFF
7	RAM2	32	0x0202 0000	0x0202 7FFF
8		32	0x0202 8000	0x0202 FFFF

4.4.3 Embedded Flash

The LGA package products of MK8000 family integrate a 512k Flash memory to store code and data. The flash communicates with the MCU through an internal SPI interface. It has the following features:

- 128 equal sectors of 4 kB each, any sector can be erased individually
- Page size 256 bytes
- Minimum 100000 erase/program cycles
- RES command, 1-byte command code
- Supports code/data encryption
- 2x1024-byte security registers with OTP locks

MK8000 also supports external flash.

4.4.4 eFuse

MK8000 integrates 1K bits eFuse memory. It is used to store the calibration/trim results and critical data. It will also enable customer to store the encryption key as well as the calibration data of applications.

Table 3 eFuse memory allocation

Function	Description	Size (Bytes)	Start Address	End Address
Reserved	Reserved	65	0x000	0x000
			0x050	0x08F
Customization	Opened for Customer	47	0x001	0x02F
	Customer Feature setting	32	0x030	0x04F

4.5 UWB Subsystem

MK8000 has integrated an 802.15.4/802.15.4z and FiRa compliant HRP UWB subsystem. It includes the following functional modules:

- A low power, wide tuning range and high dynamic range RF and analog baseband circuitry module that delivers high quality signal in different application scenarios.
- A high flexibility digital baseband modem module that supports different operation modes and options defined by standards. Advanced receiver algorithm ensures robust performance in hostile environment with all kinds of system impairments.
- A hardware/software hybrid MAC (Medium Access Control) module that is optimized for power and performance jointly.
- An LSP enhanced ranging and location module that provides high precision ranging and location capability in various applications.

The UWB subsystem is an AHB bus slave and controlled by MCU. It has a dedicated power domain and can be powered up/down separately.

4.5.1 RF module features

The RF module of UWB subsystem in MK8000 supports the following features:

- **RF top**
  - Supports 3.1 ~ 9.0GHz transmitting and receiving
  - Both TX and RX support 500MHz signal bandwidth
  - Fully integrated TRX switch
  - Integrated 50Ω matching network, enable direct antenna connection
  - Fully integrated calibration module ensures consistent performance of RF and analog circuitries
- **Transmitter**
  - The transmitter integrated a PA that can deliver up to 9dBm CW power
  - Programmable transmit output power with 30dB control range
  - Integrated power detector optimizes the output power and ensures the regulatory compliant
- **Receiver**
  - 4 dedicated RF channels enable AoA detection
  - Integrated automatic gain control can handle in band signal as high as -14dBm
  - Integrated analog filter that can reject out of band interference as high as -20dBm

4.5.2 Digital baseband modem features

MK8000 digital baseband offers high flexibility and programmability, the key features include the following:

- Supports 27.2Mbps, 6.8Mbps, 850Kbps and 110Kbps standard data rate
- Supports proprietary 54.4Mbps transmitting and receiving
- Supports SP0, SP1 and SP3 packets
- In 15.4 mode

- Supports PRF rate 15.6MHz, 62.4MHz
- Supports SFD length 8 and 64
- Payload length 0 ~ 127 bytes

- 15.4z and FiRa mode
  - Supports BPRF 62.4MHz and HPRF 124.8MHz, 249.6MHz
  - Supports SFD index 0 ~ 4
  - Payload length 0 ~ 1023 bytes
- Supports Sync PSR length 16 ~ 4096
- Supports Preamble sequence 1 ~ 32
- Supports PHR rate 110Kbps and 850Kbps
- Supports CCA mode 1~ 5
- Digital RSSI
- Integrated LQI
- Support DAA and LDC

4.5.3 MAC features

MK8000 supports the 802.15.4/15.4z/FiRa multi-standard MAC with the following features:

- Integrated 16 bits and 32 bits FCS
- Hardware based packet filter
- Packet parsing / generation
- Dedicated AES engine for authentication and data encryption/decryption
- Supports slot/non-slot CSMA/CA with multiple scan options

4.5.4 Ranging and location

MK8000 supports multiple ranging and angle measurement options:

- STS configurations
  - Number of segments 0 ~4
  - Segment length 32, 64, 128, 256
  - Also supports user defined STS sequence
  - Supports both dynamic and static STS
  - Integrated KDF, dedicated AES engine for STS
- Secured ranging
  - Basic procedure
    - SS-TWR
    - DS-TWR
  - Advanced procedures
    - Supports deferred reply time-based ranging
    - Supports fixed reply time-based ranging

    - Multi-node block-based ranging
        - Supports one to many ranging
        - Many to many ranging
- Angle measurement and location
    - PDOA
    - AOA
    - TDOA

4.6 Power Management

4.6.1 Power supply overview

MK8000 has two input supply voltage VCC and BVDD. A high efficiency buck converter is integrated which converts the input supply voltage to 1.2V VDD. There are 3 LDOs that are integrated, all of which is supplied by VDD, and generate 1.0V regulated voltage to supply function blocks, such as MCU, transmitter and receiver. Figure 4 shows the scheme of power supply in MK8000 system.

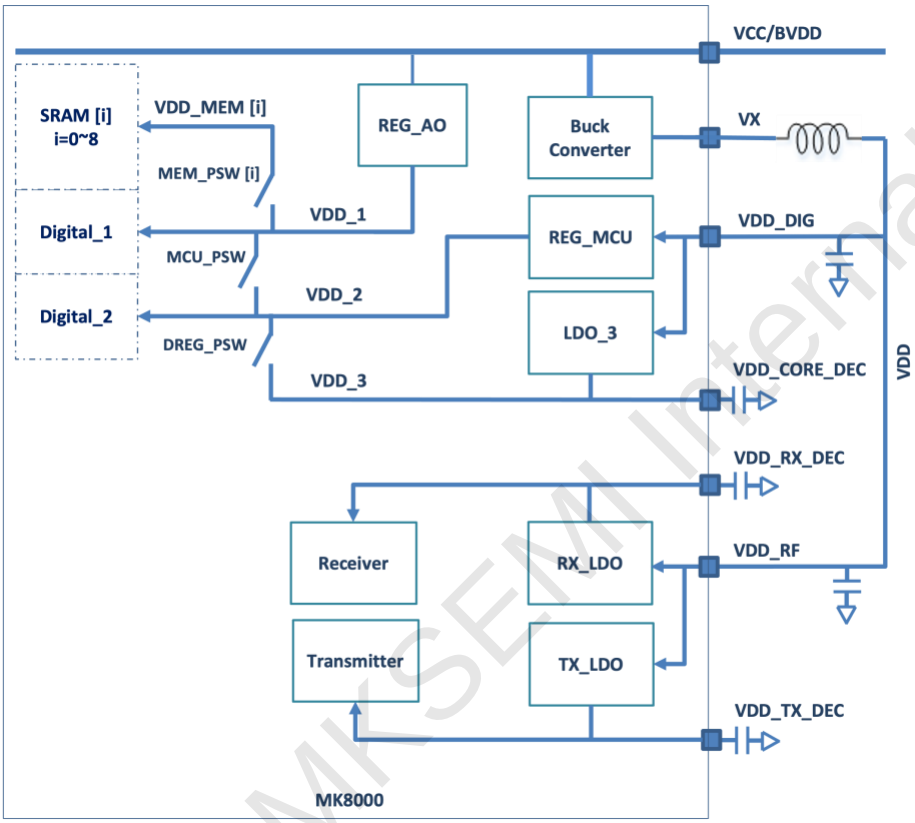


Figure 4 Power supply overview

4.6.2 MK8000 Top States and Low Power Modes

The MK8000 system has ACTIVE, TRX, SLEEP, POWER DOWN, DEEP POWER DOWN and SHELF operation states. Table 4 shows the status of major functional blocks of the system in different states.

In ACTIVE state, there are three sub-states that are defined, namely, HPACT, LPACT and ULPACT. In HPACT state, the system clock is 62.4MHz which is generated from a 38.4MHz reference clock with an internal PLL. In this state, the digital baseband supply voltage is ready for radio. In LPACT, the system clock is 48MHz generated from an internal ring oscillator, and the digital baseband supply voltage is off. In ULPACT state, the system clock is 32KHz, and the digital baseband supply voltage is off as well. Note that the 48MHz clock is not accurate enough to support radio or UART operation. If radio and/or UART is used, the 62.4MHz clock has to be used as system clock.

Table 4 States of MK8000 System

States	Radio	MCU	32KHz CLK	HCLK	NOTE
SHELF	OFF	OFF	OFF	OFF	Almost all analog and digital circuits are power off, only keep the minimum circuits are power on. The chip can exit shelf mode by reset pin, GPIO14 and GPIO17.
DEEP POWER DOWN	OFF	OFF	OFF	OFF	Retention memory and registers (SYSTEM, RTC, EFUSE, Calibration, MAC , WDT) are on, all peripherals are powered off except GPIO. The chip can be wake up by any GPIO.
POWER DOWN	OFF	OFF	ON	OFF	Retention memory and registers (SYSTEM, RTC ,EFUSE, Calibration, MAC , WDT) are on, all peripherals are powered off except GPIO, RTC, sleep timer and comparator. The chip can be woken up by any GPIO, RTC, sleep timer and comparator.
SLEEP	OFF	OFF	ON	ON	Only the CPU core sleeps, all peripherals can be active.
ACTIVE	OFF	ON	ON	ON	Radio off, MCU runs at 62.4MHz or 48MHz system clock.
TRX	ON	ON	ON	ON	Radio in active TX or RX
1. HCLK = 62.4MHz or 48MHz					

From ACTIVE state, the MCU can program the system into TRX, SLEEP, POWER DOWN, DEEP POWER DOWN or SHELF state. And in SLEEP, POWER DOWN or DEEP POWER DOWN states, external interrupt or sleep timer can be used to wake up the system into ACTIVE state through wakeup controller or NVIC. Figure 5 shows the top-level state transition of MK8000 system.

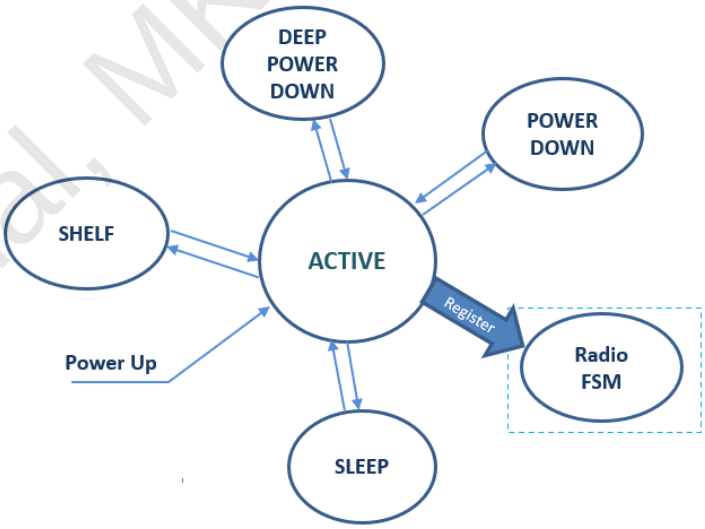


Figure 5 MK8000 Top Level FSM

4.6.3 Wakeup Controller

For the MK8000 system, waking up from DEEP POWER DOWN state is controlled by a wakeup controller. When the wakeup signal becomes valid, the PMU state machine will be reset to POWERING_UP state in which the power supply for MCU and the 48MHz RO will be turned on. After the power supply and oscillator are ready, the reset of the PMU FSM is released, and the system enters ACTIVE state.

During the wakeup, the 38.4MHz XTAL oscillator will also be powered up to reduce the power up time of the radio. When register bit MCU_WAITFOR_XRDY is asserted, the MCU clock gating will not be released until the XTAL becomes ready.

Table 5 lists the wakeup sources that are supported in MK8000. Before the system enters the DEEP POWER DOWN state, at least one of these wakeup sources needs to be enabled.

Table 5 Wakeup Sources of MK8000

Wakeup Source	Description
STIMER	Sleep time. This is wakeup source is available in Power Down mode. A wakeup event will be generated when the timer is expired. Before the system goes to Deep Power Down mode, the initial value of the counter in the timer needs to be configured.
COMP1	Comparator 1
COMP2	Comparator 2
WAKEUP_IO [17:0] [1]	Wake up IO 17:0
RTC	RTC and RTC Second interrupt

Note 1 - WAKEUP_IO will be different in different package. Only SPI0_CSn(GPIO_14) and Wake_up(GPIO_17) Pin can wakeup IC from shelf mode (low voltage to wakeup).

4.7 Reset Management Unit (RMU)

The MK8000 system Reset Management Unit (RMU) ensures proper reset operation when needed. It combines different reset sources and controls the reset lines of MK8000. An error proof reset sequence has been implemented to ensure robust startup of MK8000. In the cases when system is deadlock or malfunction, such as power supply glitches or software crash, the RMU generates reset and restart the system.

The Power-on Reset and Brown-out Reset of MK8000 provide power line monitoring with ultra-low power consumption. The source of the reset may be read from a register to help debugging.

The Reset sources in MK8000 includes POR, reset pin (RSTN pin), BOR and register bits. POR, RSTN and BOR are global signals that reset all blocks. Register bit SYS_SW_RST reset all digital blocks except for the reset generation module itself. All SOC peripherals and digital data-path have dedicated software reset signals. Table 6 lists all the reset sources in MK8000

Table 6 Reset Source in MK8000

Reset Source	Description
PORB	Power on reset signal. Reset all digital blocks when PORB is low.
RSTN	Reset signal from pin. Reset all digital blocks when RSTN is low.
BOR	Brown out detection. Reset all digital blocks when BOR is high.
SYS_SW_RST	Global reset signal from register. Reset all digital blocks except for reset generation block.
XX_SW_RST	MCU and SOC peripheral reset signals from register.
WDT	Watchdog reset

4.8 Clocks and Power Up Sequence

Figure 6 shows the timing diagram of power up sequence. The POR signal will be released when main clock and digital power supply are ready. The MCU will run the bootloader from the ROM and the application code will be fetched from the flash memory (external or internal if integrated) into the on chip SRAM and runs accordingly.

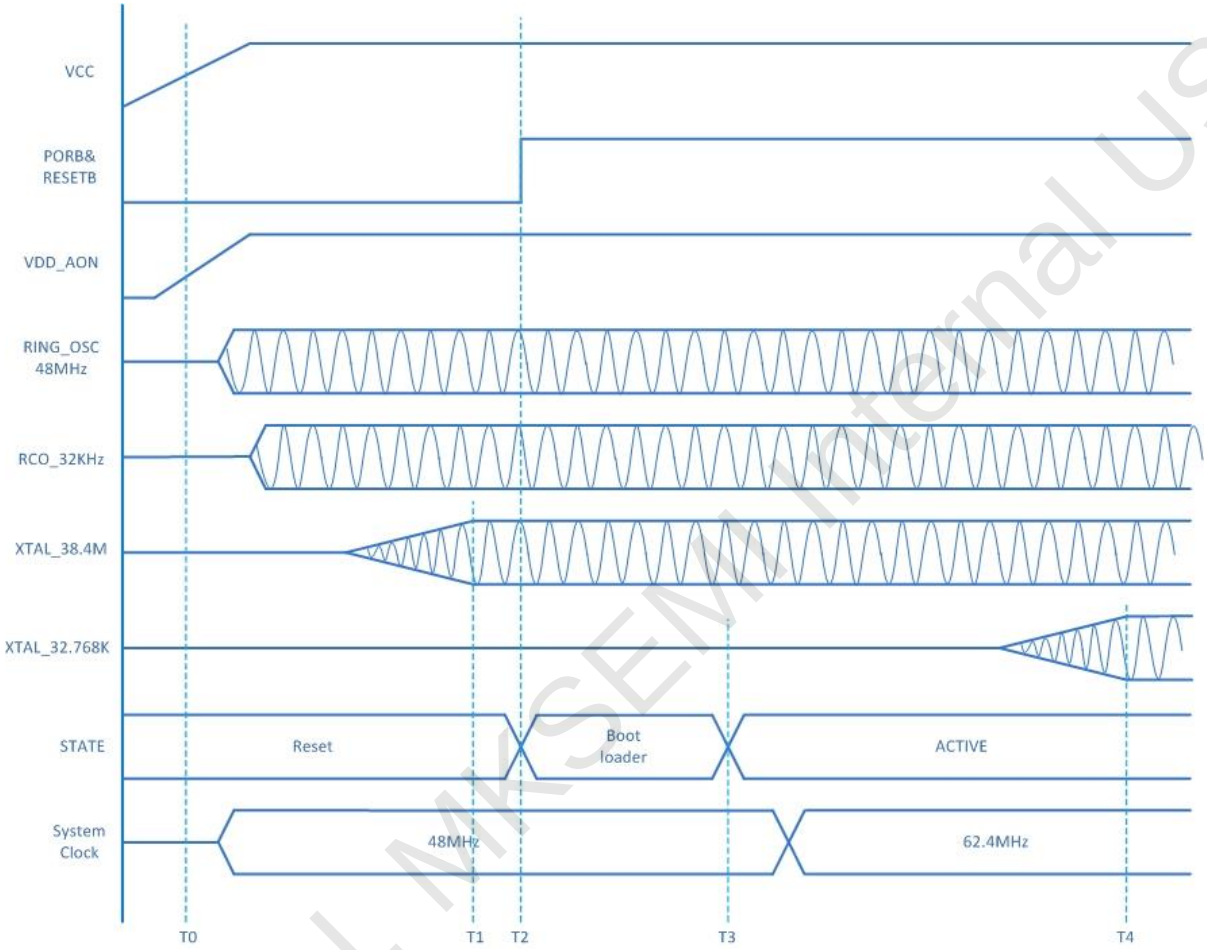


Figure 6 Timing diagram of power up sequence

Table 7 Typical Start-up timing Parameters

Parameter	Condition Description	Description	Value (µS)
T0	Typical values are T_A = 25℃ and VCC=3V	Power on reset done, guaranteed by design	2,326
T1		PoR to Ready. Depends on Crystal's feature	882
T2		Duration from PoR to IO3	12,440
T3		T3 depends on code size and whether used security encryption	8,824
T4		32.768K Crystal Power on to ready. Depends on Crystal's feature	255,242

4.9 General-purpose inputs/outputs (GPIOs)

MK8000 series products provide up to 18 GPIO pins depending on package option. Each of the GPIO pin can be configured as output (programable open/drain), or input (with or without pull-up or pull-down) or as peripheral function. Some of the GPIO pins are shared with special digital or analog functions.

Features of MK8000 GPIO includes:

- All GPIO registers are word addressable and GPIOs can be set individually.
- All GPIOs can be configured as input or output function by software.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- Direction control of individual bits.
- Programable Pull Low and Pull High mode
- Programmable driving capability in output mode
- All GPIO pins can be configured as an interrupt pin, the interrupt pin features are,
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges.
  - Level-sensitive interrupt pins can be High-active or Low-active.
- Pin interrupts can wake up the device from sleep/power down/deep power down mode, the dedicated wake-up pins can wake up the device from shelf mode
- func6 description.
  - TX_LED, RX_LED: output. Indicates that UWB TX/RX is in progress, highly valid.
  - TX_OK, RX_OK: indicates output. Indicates UWB TX/RX complete, highly valid.
  - UWB status: Output. Indicates that UWB TX or RX is being performed, highly effective.
  - SFD_LED: output. Indicates the point in time at which SFD ends, i.e. the position of the timestamp, is highly valid.
- func7 description.
  - RF_SW: Output. Used to enable off-chip TX or off-chip RX, highly effective.
  - EXPA_SW: indicates output. Used to enable off-chip PA, turned on during UWB TX, highly effective.
  - STS_SW0 to 4: Output. Indicates that the TX/RX corresponding to the STS fragment is being performed. Highly effective.

LGA40	Pin	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
5	GPIO_00	GPIO0	ADC+/CMP_P	--	--	UART1_RX	PWM_2	RX_LED	STS_SW0
6	GPIO_01	GPIO1	ADC-/CMP_N	--	SPI_Flash_D2	UART1_TX	PWM_3	TX_LED	STS_SW1
9	GPIO_02	GPIO2	V_Ref	--	SPI_Flash_D3	RTC_SYNC	PWM_4	UWB_STATUS	STS_SW2
10	GPIO_03	GPIO3	CMP_P	SPI1_CSn	SPI_Flash_CSn	I2C_SDA	PWM_0	SFD_LED	STS_SW3
11	GPIO_04	GPIO4	CMP_N	SPI1_CLK	SPI_Flash_CLK	I2C_SCL	PWM_1	RX_OK_LED	EXPA_SW
12	GPIO_05	GPIO5	Timer1_extin	SPI1_MISO	SPI_Flash_D1	UART0_TX	I2C_SDA	--	RF_SW
13	GPIO_06	GPIO6	Timer0_extin	SPI1_MOSI	SPI_Flash_D0	UART0_RX	I2C_SCL	--	EXPA_SW
14	GPIO_07	GPIO7	UART0_TX	SPI1_CLK	--	UART0_CTS	PWM_0	TX_OK_LED	STS_SW0
15	GPIO_08	GPIO8	UART0_RX	SPI1_CSn	--	UART0_RTS	PWM_1	RX_OK_LED	STS_SW1
19	GPIO_09	GPIO9	I2C_SDA	--	SPI_Flash_D3	UART1_TX	PWM_2	TX_LED	STS_SW2
20	GPIO_10	GPIO10	I2C_SCL	--	SPI_Flash_D2	UART1_RX	PWM_3	RX_LED	STS_SW3
21	GPIO_11	GPIO11	Timer1_extin	SPI0_MOSI	SPI_Flash_D1	UART1_CTS	--	--	STS_SW0
22	GPIO_12	GPIO12	Timer0_extin	SPI0_MISO	SPI_Flash_D0	UART1_RTS	--	--	STS_SW1
23	GPIO_13	GPIO13	--	SPI0_CLK	SPI_Flash_CLK	UART1_TX	--	--	STS_SW2
24	GPIO_14	GPIO14	--	SPI0_CSn	SPI_Flash_CSn	UART1_RX	--	--	STS_SW3
25	GPIO_15	SWDCLK	GPIO15	--	SPI_Flash_D2	I2C_SCL	--	--	EXPA_SW
26	GPIO_16	SWDIO	GPIO16	--	SPI_Flash_D3	I2C_SDA	--	--	RF_SW
27	GPIO_17	GPIO17	CKO_38P4M	--	--	--	Wake_Up	UWB_STATUS	EXPA_SW

Figure 7 Pin Mapping

4.10 Direct memory access controller (DMA)

MK8000 integrates a DMA controller. Table 8 lists DMA channels supported in MK8000.

DMA is used to provide a high-speed data transfer between peripherals and memory as well as from peripheral to peripheral, or from memory to memory. This keeps the MCU resources free for other operations.

The DMA controller has 8 channels in total, each one is dedicated to managing memory access requests from one or more peripherals.

Main features of the DMA controller are:

- Peripheral to Memory, Memory to Peripheral, Memory to Memory, Peripheral to Peripheral,
- All DMA channels can be configured individually:
  - Each channel is associated with either a DMA request signal coming from a peripheral, or a software trigger for memory to memory transfers. This configuration can be set by software.
  - Transfer size of source and destination are independent (byte, half-word, word).
  - Support of transfers from/to peripheral to/from memory
  - Programmable size of data to be transferred: 0 to 2^{22} - 1 bytes
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: Transfer Busy, Transfer Abort or Transfer error.

Table 8 DMA Channels

Channels	DMA Sources	
0 ~ 7	SRAM	
	AES	
	SPI Flash	
	SPI0	
	SPI1	
	Multiplex Channels	UART0
		UART1
		ADC

4.11 Nested vectored interrupt controller (NVIC)

NVIC in ARM Cortex M0 supports 32 external interrupt inputs, each with four levels of priority. It also supports both level-sensitive and pulse-sensitive interrupt lines.

Features of the NVIC,

- Low-latency interrupt processing
- 4 programmable interrupt priority levels with hardware priority level masking
- Tail-chaining, to speed up interrupt response time

4.12 Analog-to-digital converter (ADC)

4.12.1 Temperature sensor

A temperature sensor is integrated on MK8000 which has good linearity with one point calibration. The calibration data will be stored in eFuse which can be read by MCU.

4.13 True-Random-number generator (TRNG)

The MK8000 has integrated a true random number generator that can generate random keys/seeds for AES crypto engine and STS signal.

Features of the TRNG include:

- Generate interrupt when conversion is done
- Random numbers access through 4 dedicated registers

4.14 Advanced-encryption-standard (AES) engine

The AES module performs data encryption and decryption based on the standard definition. The AES engine has the following features:

- 128-bit register for storing initialization vector
- Support DMA for data load and store
- Support multiple cipher modes, ECB/CBC/CTR encryption/decryption and CCM generation-encryption and decryption-verification
- Interrupt output at the end of AES operation
- Conversion time: 42 clock cycles

4.15 Timer

MK8000 series include 4 general-purpose timers, an independent watchdog timer.

4.15.1 General-purpose timer (Timer 0 ~ Timer 1)

The general-purpose timers consist of a 32-bit auto-reload down-counter. They can be used to measure the pulse width of input signals.

Timer 0 and Timer 1 can be used for

- Input capture, and support external clock for counting and timer enable
- Support continuous operation mode only

4.15.2 General-purpose timer (Timer 2 ~ Timer 3)

The general-purpose timers consist of a 16-bit/32-bit auto-reload down-counter driven by a programable prescaler.

Pulse width and waveform periods can be modulated by using the timer prescaler. The timers are independent and do not share any resources.

Features are,

- Timer2 and Timer3 support 1/16/256 prescaler
- Support Free Running, Continuous and One-Shot modes

4.15.3 Watchdog timer (WDT)

A countdown watchdog timer using the low frequency clock source offers configurable and robust protection against application lock-up. The WDT resets the system when software fails to clear the WDT within the selected time interval. It can operate in TRX, ACTIVE and SLEEP mode

Features include:

- Programmable 32-bit timer
- Internally resets the chip if not reload periodically
- Flag to indicate watchdog reset

4.15.4 Sleep Timer

Sleep timer has a 32-bit downward counter which has the following features:

- Wakeup the system from SLEEP and POWER DOWN mode
- Generate an interrupt signal when counter reaches 0

4.16 Pulse-Width Modulation (PWM)

5 PWM channels are supported in MK8000. Each channel has dedicated registers to configure duty cycle, and period. PWM 0/1/2/3 can configure its phase dependently. The period of the PWM in different counter length mode can be calculated by the follow equation:

Period = Tclk * (PWMGPS +1)*（PWMxPS +1）* 256

4.17 Real-time clock (RTC)

RTC has a 32-bit upward counter, RTC support following features:

- Programmable 32-bit match compare register
- Generates an interrupt when RTC value and compare registers are identical
- Wake up MCU from low power mode
- Alert in every second

4.18 Inter-integrated circuit interface (I^2C)

MK8000 has integrated I^2C interface to enable the communication between the MK8000 and the external devices. Each device on the I^2C interface can be recognized by a unique address and operates as either a receiver-only device or a transmitter with the capability of both sending and receiving the information. The I^2C is a multi-master bus and can be controlled by more than one bus master.

MK8000 I^2C interface enables the following features:

- Supports 100 Kbit/s, 400 Kbit/s
- Supports Master and Slave functions
- Multiple I^2C slave address supported in hardware
- 7-bit and 10-bit addressing mode
- Programmable setup and hold times
- TX_FIFO and RX_FIFO have an independent buffer size with 8-Byte depth in both master and slave modes
- Support clock stretching in slave mode
- Programmable digital noise filters

4.19 Universal Asynchronous Receiver Transmitter (UART)

MK8000 integrates two UART ports with the following features:

- Full-duplex operation
- Programmable baud rate with the maximum rate of 2Mbps
- Programmable data length (5-8 bits), parity (with odd, even select or Stick Parity), and stop bit length (1/1.5/2)
- FIFO size up to 16 Bytes
- Auto CTS and RTS serial data flow control
- DMA supported

4.20 Serial peripheral interface (SPI)

MK8000 integrates two SPI interfaces that support the following features:

- Support Master mode runs up to 31.2Mbits/s
- Support Slave mode runs up to 5.2Mbit/s
- Full-duplex synchronous transfer
- Separate transmit and receive FIFO memory buffers, with 8 data entries in 16 bits
- 4~16-bit data size selection
- Configurable SPI Polarity and Phase
- Support DMA

4.21 Clock output

MK8000 can output 38.4MHz/48MHz/32.768K/32K clock.

4.22 Serial Wire Debug Port (SWD)

- An Arm SW debug interface is provided to allow a serial wire debugging, its features are
- Support 4 breakpoints and 2 watchpoints.
- Support processor halt, single-step
- Support processor core register access
- Can Reset and HardFault Vector Catch,
- Unlimited software breakpoints, and full system memory access

5. Specifications and Characteristics

5.1 Electrical Characteristic

Table 9 Recommended operation condition and electrical characteristic

(Typical values are T_A = 25℃ and VCC=3V).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		1.8	3.0	3.6	V
V_{BVDD}	Supply Voltage for internal DC/DC and IO		1.2	3.0	3.6	V
$V_{VDD\ RF}$	Supply Voltage for RF		1.1	1.2	3.6	V
$V_{VDD\ AN}$	Supply Voltage for analog		1.1	1.2	3.6	V
T_A	Operating Temperature		-40	+25	+85	℃
ESD	HBM			4000		V
	CDM			1000		

Table 10 Current Characteristic (Typical values are T_A = 25℃ and VCC=3V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{VCC_LPACT}	Current dissipation in low performance active mode	Vcc = 3V, DC-DC ON [1]		1.2		mA
		Vcc = 3V, DC-DC OFF [1]		2.6		mA
		Vcc = 1.8V, DC-DC ON [1]		1.7		mA
		Vcc = 1.8V, DC-DC OFF [1]		2.4		mA
$I_{VCC\_MCU\_LPACT}$	MCU current dissipation in low performance active mode	Vcc = 3V, DC-DC ON [1]		24.1		µA/MHz
		Vcc = 3V, DC-DC OFF [1]		54.3		µA/MHz
		Vcc = 1.8V, DC-DC ON [1]		36.0		µA/MHz
		Vcc = 1.8V, DC-DC OFF[1]		49.7		µA/MHz
I_{VCC_HPACT}	Current dissipation in high performance active mode	Vcc = 3V, DC-DC ON [2]		3.8	5.4	mA
		Vcc = 3V, DC-DC OFF [2]		8.1	11.5	mA
		Vcc = 1.8V, DC-DC ON [2]		5.8		mA
		Vcc = 1.8V, DC-DC OFF[2]		8.1		mA
$I_{VCC\_MCU\_HPACT}$	MCU current dissipation in high performance active mode	Vcc = 3V, DC-DC ON [2]		59.1		µA/MHz
		Vcc = 3V, DC-DC OFF [2]		134.1		µA/MHz
		Vcc = 1.8V, DC-DC ON [2]		92.3		µA/MHz
		Vcc = 1.8V, DC-DC OFF [2]		130.4		µA/MHz
$I_{VCC\_SLEEP\_LP}$	Current dissipation in low performance sleep mode	Vcc = 3V, DC-DC ON [1]		0.9		mA
		Vcc = 3V, DC-DC OFF [1]		1.9		mA
		Vcc = 1.8V, DC-DC ON [1]		1.3		mA
		Vcc = 1.8V, DC-DC OFF [1]		1.7		mA
$I_{VCC\_MCU\_SLEEP\_LP}$	MCU current dissipation in low performance sleep mode	Vcc = 3V, DC-DC ON [1]		18.1		µA/MHz
		Vcc = 3V, DC-DC OFF [1]		40.0		µA/MHz
		Vcc = 1.8V, DC-DC ON [1]		26.3		µA/MHz
		Vcc = 1.8V, DC-DC OFF [1]		36.2		µA/MHz
$I_{VCC\_SLEEP\_HP}$	Current dissipation in high performance sleep mode	Vcc = 3V, DC-DC ON [1]		3.1	4.8	mA
		Vcc = 3V, DC-DC OFF [1]		6.8	10.5	mA
		Vcc = 1.8V, DC-DC ON [1]		4.9		mA
		Vcc = 1.8V, DC-DC OFF [1]		7.0		mA
$I_{VCC\_MCU\_SLEEP\_HP}$	MCU current dissipation in high performance sleep mode	Vcc = 3V, DC-DC ON [1] -		50.4		µA/MHz
		Vcc = 3V, DC-DC OFF [1]		113.2		µA/MHz
		Vcc = 1.8V, DC-DC ON [1]		78.2		µA/MHz
		Vcc = 1.8V, DC-DC OFF [1]		111.5		µA/MHz

I_{VCC_DPD}	Current dissipation in deep power down mode	Vcc = 3V		2.4	6	µA
		Vcc = 1.8V		6.9		µA
I_{VCC_PD}	Current dissipation in power down mode	Vcc = 3V		3.3	7	µA
		Vcc = 1.8V		7.9		µA
$I_{VCC\text{-}SHELF}$	Current dissipation in shelf mode	Vcc = 3V		331.2	500	nA
		Vcc = 1.8V		82.0		nA
Channel 2 Current Consumption						
I_{TX_CH2}	TX peak current	Vcc = 3.0V, Pout = -41.3dBm/MHz, DC/DC on		16.7		mA
		Vcc = 3.0V, Pout = -41.3dBm/MHz, DC/DC off		38.4		mA
		Vcc = 1.8V, Pout = -41.3dBm/MHz, DC/DC on		27.3		mA
		Vcc = 1.8V, Pout = -41.3dBm/MHz, DC/DC off		38.0		mA
I_{RX_CH2}	RX peak current (Low Power Mode)	Vcc = 3.0V, DC/DC on		42.2		mA
		Vcc = 3.0V, DC/DC off		101.8		mA
		Vcc = 1.8V, DC/DC on		69.2		mA
		Vcc = 1.8V, DC/DC off		100.0		mA
	RX peak current (High Performance Mode)	Vcc = 3.0V, DC/DC on		49.3		mA
		Vcc = 3.0V, DC/DC off		117.1		mA
		Vcc = 1.8V, DC/DC on		80.8		mA
		Vcc = 1.8V, DC/DC off		115.8		mA
Channel 5 Current Consumption						
I_{VCC_Cap}	TX peak current	VCC connect to 47µF external Capacitor, DC/DC is on [2]			10	mA
	RX peak current				10	
I_{TX_CH5}	TX peak current	Vcc = 3.0V, Pout = -41.3dBm/MHz, DC/DC on		17.0		mA
		Vcc = 3.0V, Pout = -41.3dBm/MHz, DC/DC off		39.4		mA
		Vcc = 1.8V, Pout = -41.3dBm/MHz, DC/DC on		27.7		mA
		Vcc = 1.8V, Pout = -41.3dBm/MHz, DC/DC off		39.0		mA
I_{RX_CH5}	RX peak current (Low Power Mode)	Vcc = 3.0V, DC/DC on		43.5		mA
		Vcc = 3.0V, DC/DC off		104.6		mA
		Vcc = 1.8V, DC/DC on		71.2		mA
		Vcc = 1.8V, DC/DC off		103.6		mA
	RX peak current	Vcc = 3.0V, DC/DC on		52.8		mA
		Vcc = 3.0V, DC/DC off		125.8		mA

	(High Performance Mode)	Vcc = 1.8V, DC/DC on		85.9		mA
		Vcc = 1.8V, DC/DC off		124.5		mA
Channel 9 Current Consumption						
I_{VCC_Cap}	TX peak current	VCC connect to 47µF external Capacitor, DC/DC is on [2]			10	mA
	RX peak current				10	mA
I_{TX_CH9}	TX peak current	Vcc = 3.0V, Pout = -41.3dBm/MHz, DC/DC on		18.0		mA
		Vcc = 3.0V, Pout = -41.3dBm/MHz, DC/DC off		41.9	48	mA
		Vcc = 1.8V, Pout = -41.3dBm/MHz, DC/DC on		29.6		mA
		Vcc = 1.8V, Pout = -41.3dBm/MHz, DC/DC off		41.5		mA
I_{RX_CH9}	RX peak current (Low Power Mode)	Vcc = 3.0V, DC/DC on		43.4		mA
		Vcc = 3.0V, DC/DC off		106.1		mA
		Vcc = 1.8V, DC/DC on		72.6		mA
		Vcc = 1.8V, DC/DC off		104.9		mA
I_{RX_CH9}	RX peak current (High Performance Mode)	Vcc = 3.0V, DC/DC on		52.2		mA
		Vcc = 3.0V, DC/DC off		124.4	139	mA
		Vcc = 1.8V, DC/DC on		84.8		mA
		Vcc = 1.8V, DC/DC off		123.1		mA

1. MCU runs Drystone from SRAM, HCLK = 48MHz
2. MCU runs Drystone from SRAM, HCLK = 62.4MHz
3. Test Conditions (in T/RX Mode): Preamble = 64 Ci = 9, SFD = 8(2# in 802.15.4z), Payload length = 20bytes, Data Rate = 6.8Mbps, Carrier frequency offset = ±1 ppm, 10Hz
4. VDDCORE=02, ADC=2G, port=0

5.2 UWB Specification and Performance

5.2.1 UWB Specification and Performance

Table 11 UWB specification and Performance

(Typical values at T_A = 25℃ and VCC=3V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
F_{RF}	Frequency range		3.1		9	GHz
T_{CF}	Carrier Frequency Tolerance		-15		+15	ppm
BW_{RF}	Supported signal bandwidth			499.2		MHz
P_{TX}	Transmitter output power range	CH5		28.5		dB
		CH9		25.0		dB

P_{TX_MAX}	Maximum transmitter CW output power	CH2		10.81	11.33	dBm
		CH5		10.85	11.43	dBm
		CH9		8.93	9.19	dBm
P_{TX_MIN}	Minimum transmitter CW output power	CH2	-20.42	-19.01		dBm
		CH5	-17.31	-14.69		dBm
		CH9	-19.61	-16.07		dBm
P_{TX_ERR}	PA output level error[1]	PA output level error when power detector auto-calibration is on			1.5	dB
G_{FSTEP}	PA fine gain step	CH5				dB
		CH9		0.47		dB
Δ_{GF_MAX}	PA fine gain step error	CH5				dB
		CH9		0.47		dB
Δ_{GF_MIN}		CH5				dB
		CH9		-0.32		dB
PSD_{FCC}	Transmit spectrum mask	325MHz<|f-fc|<400MHz |f-fc|>400MHz at channel 9			-10 -18	dB
PSD_{MAX}		325MHz<|f-fc|<400MHz |f-fc|>400MHz at channel 9			-10 -18	dB
P_{SPUR}	Transmit spurious level			0		dB
T_{PT}	Pulse timing tolerance		-15	0	+15	ppm
T_{RS}	Pulse rising time	Pulse monotonically rises to the peak value at channel 5		1.42		ns
		Pulse monotonically rises to the peak value at channel 9		1.44		ns
T_{MAIN}	Main lobe duration of TX pulse cross correlation	Main lobe is the portion of cross correlation with magnitude at least 0.8 at channel 9		1.41		ns
V_{SIDE}	Side lobe magnitude	Normalized cross correlation sidelobe at channel 9		14.7	30	%
ER_{SHR}	NRMSE of SHR part	CH9		19.4	25	%
ER_{STS}	NRMSE of STS part			13.4	25	%
ER_{PHR}	NRMSE of PHR part			24.1	30	%
ER_{PL}	NRMSE of PHR part			23.7	30	%
AV_{PL}	The pulse level difference	Average level difference of SHR, PHR, STS, PSDU	-2	0.6	2	dB
Sensitivity[2] (Normal mode)	850Kbps	CH2, 1% PER, CFO 1ppm		-99.8		dBm
	6.8Mbps - BPRF			-92.3		
	850Kbps	CH2, 10% PER, CFO 10ppm				
	6.8Mbps - BPRF					
	850Kbps	CH5, 1% PER, CFO 1ppm				
	6.8Mbps - BPRF			-94.4		
	850Kbps	CH5, 10% PER, CFO 10ppm				
	6.8Mbps - BPRF					
	850Kbps	CH9, 1% PER, CFO 1ppm				
	6.8Mbps - BPRF			-92.3		
	850Kbps	CH9, 10% PER, CFO 10ppm				
	6.8Mbps			-92.3		
Sensitivity[2] (High Performance mode)	850Kbps	CH2, 1% PER, CFO 1ppm		-100.5		dBm
	6.8Mbps - BPRF			-93.7		
	850Kbps	CH2, 10% PER, CFO 10ppm				
	6.8Mbps - BPRF			-95.2		
	850Kbps	CH5, 1% PER, CFO 1ppm				
	6.8Mbps - BPRF			-95.6		
	850Kbps	CH5, 10% PER, CFO 10ppm				

	6.8Mbps - BPRF					
	850Kbps	CH9, 1% PER, CFO 1ppm				
	6.8Mbps - BPRF			-93.4		
	850Kbps	CH9, 10% PER, CFO 10ppm				
	6.8Mbps - BPRF			-93.9		
RX_{MAX_850K}	Maximum received UWB signal level	CH9,500MHz bandwidth		-14.8		dBm
$RX_{MAX\_6.8M}$				-14.5		dBm
Int_{OOB}	OOB Interference rejection	Blocking 3300MHz<f≤ 4200MHz, CH9		-31.3		dBm
		Blocking 5725MHz<f≤ 5850MHz, CH9		-30		dBm
		Blocking 5925MHz<f≤ 7125MHz, CH9	-40.8	-39		dBm
R_Δ	Ranging accuracy	LOS condition, TRX spacing 3m	-10		10	cm
DR_{fp}	First path dynamic range		20			dB
F_{ACC}	Angle accuracy	LOS condition, TRX spacing 3m, 3σ	-3		3	degree

1. Measured at the maximum level allowed by FCC
2. Test Conditions in T/RX mode are Preamble = 64, Ci =9, SFD #2, Payload length = 20bytes,
3. The sensitivity value for CH2 is measured at port = 2, CH5/CH9 is measured at port =3;

5.2.2 Timing Requirements

Table 12 UWB Timing specification

(Typical values are T_A = 25℃ and VCC=3V)

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
$bt_{Tolerance}$	block timing tolerance		-100	--	100	ppm
AC_{tr}	Tround and Treply accuracy		-15		15	ppm
$TR_{tr\text{-}start}$	The start of transmission time [1]		0		+10	μs
$t_{RX\text{-}TX}$	Turnaround time RX to TX		7.7	7.46	12	μs
$t_{TX\text{-}RX}$	Turnaround time TX to RX		7.5	7.24	12	μs
$T_{ACT\text{-}RAD}$	Switching time from high performance active to radio time, without PA power calibration			23		μs

1. The start time according to the position of the start of the reference CM or RIM within their slots.
2. PHY derives the clock used for measuring Tround and Treply from the same clock reference as the TX carrier and pulse clock.

5.3 Reference clock

5.3.1 Main clock

Table 13 38.4-MHz Crystal Oscillator Reference Clock

(Typical values are TA = 25℃ and VCC=3V)

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
F_{xtal-H}	Crystal frequency(1)			38.4		MHz
△f	Crystal accuracy		-15		+15	ppm
C_L	Crystal load capacitance		5	8	15	pF
ESR	Equivalent Series Resistance			40	100	Ω
T_{start}	Start-up time	VCC = 3V		476.0		µs
		VCC = 1.8V		509.0		µs
I_{start}	Start-up current	VCC = 3V		849.0		µA
		VCC = 1.8V		830.0		µA
38.4MHz External Clock(1)	Amplitude, OSC_IN input pin	High Level Voltage	1		Vcc	V
		Low Level Voltage	GND		0.2	
	SSB Phase noise power density	1 kHz offset		-130		dBc/Hz
		10 kHz offset		-140		
	Duty Cycle		40		60	%
$A_{SIN\_MIN\_XTAL}$	38.4MHz minimum acceptable sine wave input	VCC = 1.7V	493.1		1200	mV
		VCC = 1.8V	486.6		1200	mV
		VCC = 3V	492.8		1200	mV
		VCC = 3.6V	493.4		1200	mV
$A_{SQ\_MIN\_XTAL}$	38.4MHz minimum acceptable square wave input	High Level Voltage VCC = 1.7V	1200			mV
		Low Level Voltage VCC = 1.7V			100	mV
		High Level Voltage VCC = 1.8V	1200			mV
		Low Level Voltage VCC = 1.8V			100	mV
		High Level Voltage VCC = 3V	1200			mV
		Low Level Voltage VCC = 3V			100	mV
		High Level Voltage VCC = 3.6V	1200			mV
		Low Level Voltage VCC = 3.6V			100	mV
1. MK8000 accepts external 38.4-MHz clock input						

Table 14 48Mhz Ring Oscillator Reference Clock

(Typical values are TA = 25℃ and VCC =3V)

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Oscillator frequency	VCC = 3V & 1.8V	-2.5%	48 (1)	+2.5%	MHz
TC		VCC = 3V		0.011		%/℃

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
	Temperature Coefficient	VCC = 1.8V		0.016		%/℃
t_{start}	Start-up time			3		µs
1.After calibrated with external crystal						

5.3.2 Low frequency clock

Table 15 32.768-kHz Crystal Oscillator Reference Clock

(Typical values are T_A = 25℃ and VCC=3V)

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
Fxtal-L	input frequency			32.768		kHz
$\triangle_{XTAL32}$	Crystal tolerance		-50		+50	ppm
ESR	Equivalent serial resistance				100	kΩ
CL	load capacitance		5		12	pF
Tstart	Start-up time	VCC = 3V		0.16		s
		VCC = 1.8V		0.17		s
32.768kHz External Clock(1)	Amplitude, OSC_O input pin	High Level Voltage	1		Vcc	V
		Low Level Voltage	GND		0.2	
	Duty Cycle		40		60	%
$A_{SQ\_MIN\_XTAL}$	32.768KHz minimum acceptable square wave input	High Level Voltage VCC = 1.7V	90% * V_{BVDD}		V_{BVDD}	mV
		Low Level Voltage VCC = 1.7V			10% * V_{BVDD}	mV
		High Level Voltage VCC = 1.8V	90% * V_{BVDD}		V_{BVDD}	mV
		Low Level Voltage VCC = 1.8V			10% * V_{BVDD}	mV
		High Level Voltage VCC = 3V	90% * V_{BVDD}		V_{BVDD}	mV
		Low Level Voltage VCC = 3V			10% * V_{BVDD}	mV
		High Level Voltage VCC = 3.6V	90% * V_{BVDD}		V_{BVDD}	mV
		Low Level Voltage VCC = 3.6V			10% * V_{BVDD}	mV
$A_{SIN\_MIN\_XTAL}$	32.768KHz minimum acceptable sine wave input	VCC = 1.7V	290		1200	mV
		VCC = 1.8V	290		1200	mV
		VCC = 3V	290		1200	mV
		VCC = 3.6V	290		1200	mV
1. MK8000 accepts external 32.768-kHz clock input						

Table 16 32.768KHz RC Oscillator Reference Clock

(Typical values are T_A = 25℃ and VCC =3V).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Oscillator frequency	VCC = 3V & 1.8V	-1.5%	32.768 (1)	+1.5%	kHz
TC	Temperature Coefficient	VCC = 3V		0.009		%/℃
		VCC = 1.8V		0.009		%/℃
$t_{startup}$	Start-up time	VCC = 3V		193		µs
		VCC = 1.8V		238		µs
1.After calibrated with external crystal						

5.4 Power-up timing Parameters

Table 17 Power-up from Sleep/Deep Sleep mode

(Typical values are T_A = 25℃ and VCC=3V).

	Active	Sleep	Deep Power Down
Time to MCU Ready with external Clock	--	<1us	<4 µs
Time to Tx/Rx Ready with external Clock	30µs	<31 µs	<120 µs
Time to MCU Ready with external Crystal	--	<1 µs	<4 µs
Time to Tx/Rx Ready with external Crystal	30µs	<31 µs	<500 µs

Note, the time will be 20us longer if PA power calibration is running during radio sequence.

5.4.1 BOD/BOR Parameters

This device has the integrated power-on reset (POR)/power-down reset (PDR), coupled with a brown-out reset (BOR) circuit. Details please see below table,

Table 18 BOR Parameters

(Typical values are T_A = 25℃ and VCC=3V).

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(3)	Reset temporization after BOR0 is detected	V_{CC} rising			5	µs
V_{BOR0}	Brown-out reset threshold 0	Rising edge	1.655	1.684	1.705	V
		Falling edge	1.630	1.653	1.670	
V_{BOR1}	Brown-out reset threshold 1	Rising edge		2.037		V
		Falling edge		2.010		
V_{BOR2}	Brown-out reset threshold 2	Rising edge		2.240		V
		Falling edge		2.211		
V_{BOR3}	Brown-out reset threshold 3	Rising edge		2.546		V
		Falling edge		2.513		
V_{hyst_BOR}	Hysteresis voltage of BORH(except BORH0)	Low	10	31.64	50	mV
		Medium		142.66		
		High		244.58		
I_{DD} (BOR)(2)	Current dissipation of BOR			31		µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. The BOR current is important, if in sleep and deep sleep mode, SRAM's retention current can meet customer's requirements, the code in SRAM doesn't need reload again from flash. In these case, BOR's current is important, especially for BOR0.
3. Data reference simulation result < 5us

Table 19 BOD Parameters

(Typical values are T_A = 25℃ and VCC=3 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOD0}	Brown-out detect threshold 0 in normal	Rising edge	1.805	1.825	1.855	V
		Falling edge	1.695	1.716	1.745	
V_{BOD1}	Brown-out detect threshold 1 in normal	Rising edge				V
		Falling edge				
V_{BOD2}	Brown-out detect threshold 2 in normal	Rising edge				V
		Falling edge				
V_{BOD3}	Brown-out detect threshold 3 in normal	Rising edge				V
		Falling edge				
V_{BOD4}	Brown-out detect threshold 4 in normal	Rising edge				V
		Falling edge				
V_{hyst_BOD}	Hysteresis voltage of BOD	Disable		1		mV
		Normal	90	109.4	130	mV
		High		198		mV

5.5 Temperature and Battery Voltage Monitors

Temperature sensor has to be calibrated (refer to **Error! Reference source not found.**) to obtain good overall accuracy of the temperature measurement. Each device is individually factory-calibrated by MK Semi. The temperature sensor factory calibration data are stored by MK Semi in the system memory area, accessible in read-only mode.

Table 20 Temperature Sensor characteristics

(Typical values are T_A = 25℃ and VCC=3V).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
T_m(℃)	Temperature sensor range		-40		85	℃
dT_m(℃)	Temperature sensor accuracy	After calibration at 25℃ (±0.5℃)				
t_{START} (TS_BUF)	Sensor buffer start-up time in continuous mode(1)					µs
I_{TS}	Temperature sensor consumption from V_{DD_AN}, when selected by ADC	VCC = 3V		662.33		µA
		VCC = 1.8V		635.33		µA
t_{R_temp}	ADC sampling time when reading the temperature，CLK：62.4MHz ADC rate：160Khz Sample = 64	VCC = 3V		455		µs
		VCC = 1.8V		418.66		µs
	ADC sampling time when reading the temperature，CLK：62.4MHz ADC rate：160Khz Sample = 8	VCC = 3V		52.31		µs
		VCC = 1.8V		58.10		µs

Note, 1. Continuous mode means TRX/MCU/IDLE modes, or temperature sensor enable in sleep mode

This embedded hardware enables the application to measure the VBAT battery voltage using the internal ADC channel. As the VBAT voltage may be higher than the VCC, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3[(2)]. As a consequence, the converted digital value is one third of the VBAT voltage.

Table 21 V_{BAT} Monitoring Characteristics

(Typical values are T_A = 25℃ and VCC=3V).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
BAT_m	Battery monitor range[(1)]		1.8		3.6	V
B_m-step	Battery monitor accuracy			26.7		mV
Er[(2)]	Error on V			0.01		%
I_{VS}	Battery monitor consumption from V_{CC}, when selected by ADC	VCC = 3V		455.0		µA
		VCC = 3V		418.7		µA
t_{S_vbat}	ADC sampling time when reading V_{BAT}, CLK: 62.4MHz ADC rate; 200Khz Sample = 1	VCC = 3V		5.0		µs
		VCC = 1.8V		5.0		µs

Note,

1, This range is used if we can integrate the VBAT detect circuit internally. So V_{CC} pin will be directly connected to Battery.

2. Guaranteed by design

5.6 I/O Characteristics

5.6.1 General

Table 22 I/O static characteristics

(Typical values are T_A = 25℃ and VCC=3V)

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
GPIOs	High source current	Current @2.7V~3.6V, $V_{OH} = V_{BVDD} – 0.3V$		13.3		mA
		Current @1.8V ~ 2.7V, VOH = VBVDD – 0.3V		8.7		mA
	Normal source Current	Current @2.7V~3.6V, VOH = VBVDD – 0.3V		1.0		mA
		Current @2.7V~3.6V, VOH = VBVDD – 0.3V		0.8		mA
	High sink Current	Current @2.7V~3.6V, VOL = 0.3V		19.0		mA
		Current @1.8V ~ 2.7V, VOL = 0.3V		12.6		mA
	Normal sink Current	Current @2.7V~3.6V, VOL = 0.3V		0.9		mA
		Current @1.8V ~ 2.7V, VOL = 0.3V		0.8		mA
V_{OH}	High level output voltage		$0.9 \times V_{BVDD}$		V_{BVDD}	V

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage		0		0.1× V_{BVDD}	V
V_{IH}	High level input voltage		0.7 × V_{BVDD}			V
V_{IL}	Low level input voltage		-0.5		0.3 × V_{BVDD}	V
R_{PH_PL}	Resister in pull up mode in different setting (week driver capability)	IO input is enable. IO_PHI[2:0] = 3'b001		143@3V 296@1.8V		KΩ
		IO_PHI[2:0] = 3'b010		25.6		
		IO_PHI[2:0] = 3'b011.		11.74		
		IO_PHI[2:0] = 3'b100.		6.55		
		IO_PHI[2:0] = 3'b101.		1.63		

5.6.2 Reset pin input characteristics

A Low on this pin can reset the device, then make all the I/O ports and peripherals to their default states, and the bootloader will load code to RAM to execute.

Table 23 Reset pin characteristics

(Typical values are T_A = 25°C and VCC=3V)

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL(Reset)}$	Reset pin input low voltage				0.3 x V_{BVDD}	V
$V_{IH(Reset)}$	Reset pin input high voltage		0.7 x V_{BVDD}			V
$V_{hys(Reset)}$	Reset pin trigger voltage hysteresis	VCC = 3V	480	543.5	560	mV
		VCC = 1.8V		368		mV
R_{PR}	Pull up resister value in reset	VCC = 3V		138.54		KΩ
		VCC = 1.8V		283.31		KΩ
HTN_{Reset}	Low voltage hold time in reset mode	VCC = 3V		8.04		ms
		VCC = 1.8V		17.00		ms

Note, Reset Pin should connect a 0.1uF capacitor to ground, and this capacitor should be placed as close as possible to Reset pin. And a filter is connected after the Schmitt trigger, the filter can filter the pulse width of spikes or glitches of 3~20ns.

5.6.3 SPI

Table 24 SPI characteristics

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SPI clock frequency	Master mode, 1.8V~3.6V			31.2	MHz
		Slave mode, 1.8V~3.6V			5.2	
$t_{su(CSn)}$	CSn setup time	Slave mode, SPI prescaler = 2	6 x 16			ns
$t_{h(CSn)}$	CSn hold time	Slave mode, SPI prescaler = 2	6 x 16			ns
$t_{w(SCKH)}$	SCK high time	Master mode				ns
$t_{w(SCKL)}$	SCK low time	Master mode				ns

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su(MI)}$	Master data input setup time					ns
$t_{su(SI)}$	Slave data input setup time		5 x 16			ns
$t_{h(MI)}$	Master data input hold time					ns
$t_{h(SI)}$	Slave data input hold time		5 x 16			ns
$t_{a(SO)}$	Data output access time	Slave mode		48.9		ns
$t_{dis(SO)}$	Data output disable time	Slave mode				ns
$t_{v(SO)}$	Slave data output valid time	1.8V~3.6V		87.8		ns
$t_{v(MO)}$	Master data output valid time					ns
$t_{h(SO)}$	Slave data output hold time	Slave mode (after enable edge)		56.2		ns
$t_{h(MO)}$	Master data output hold time	Master mode (after enable edge)				ns
$t_{r(SCK)}$	Raise time			39.8		ns
$t_{f(SCK)}$	Fall time			40.5		ns

Note,
1. IO Driver configuration 0 (week driver capability)

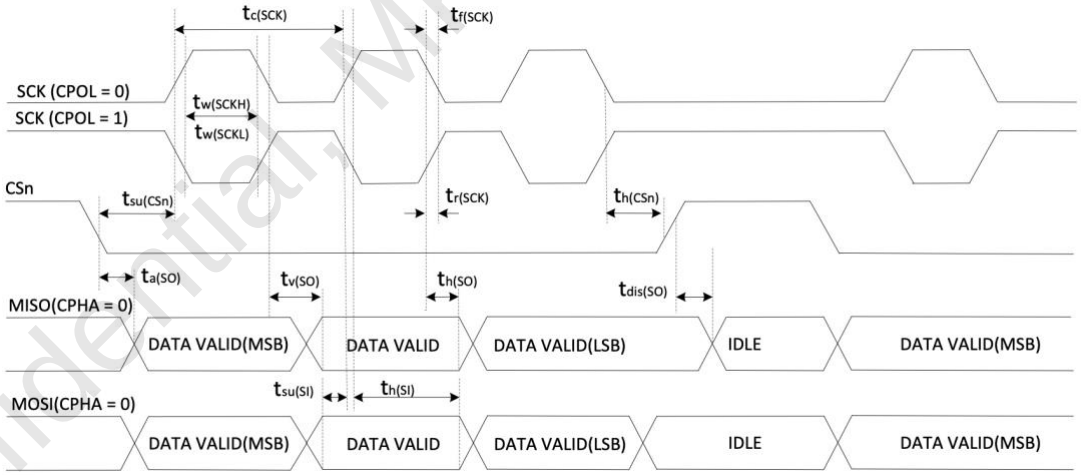


Figure 8 SPI timing diagram slave mode, CPHA = 0

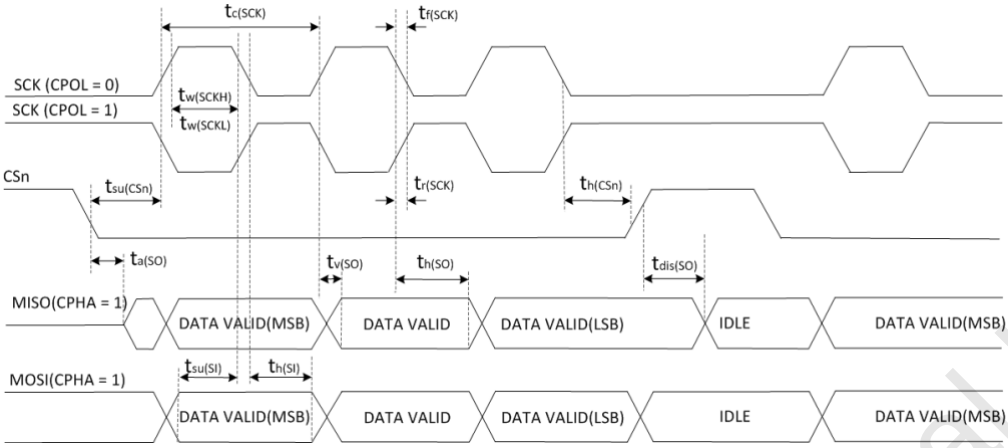


Figure 9 SPI timing diagram slave mode, CPHA = 1

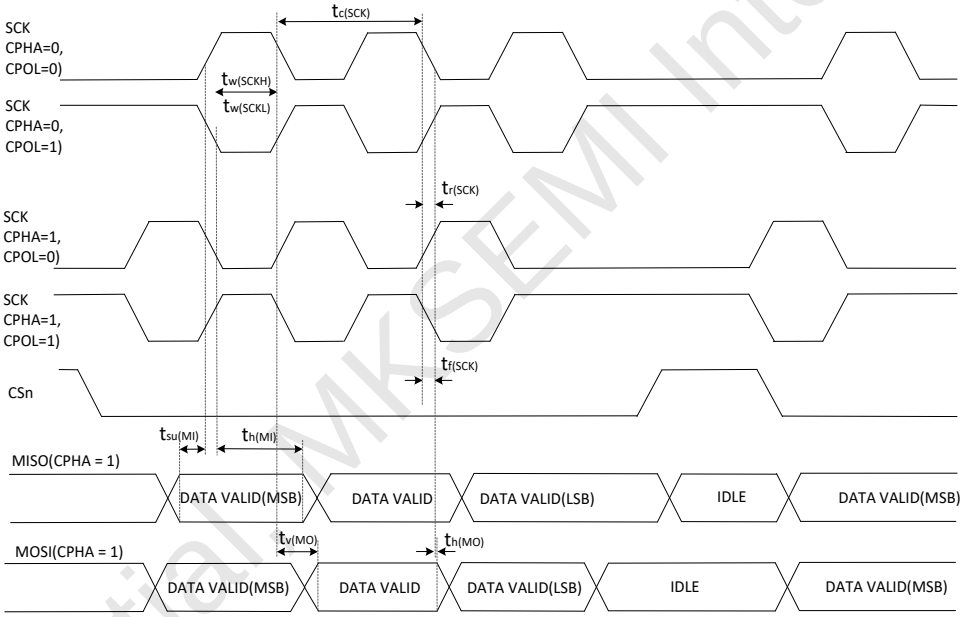


Figure 10 SPI timing diagram - master mode

5.6.4 I2C

I2C support analog and digital noise filter, both noise filter can be configured by register for SDA and SCL port. The digital noise filter step can be 1 t_{I2C_CLK}. I2C feature details please refer to I2C feature details.

Table 25 I2C feature details

(Typical values are T_A = 25°C and VCC=3V).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
I_{Drive}	Control the current sink capability of the pins	For Standard and Fast mode		0.95		mA
f_{I2C}	Filter in I2C (configurable)	Glitch filter in fast mode	0		50	ns

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Normal mode			100		kHz
	Fast mode			400		
t_f	Fall time of both SDA and SCL signals	Standard mode		3.7		ns
		Fast mode		3.6		
t_r	Rise time of both SDA and SCL signals	Standard mode		91		ns
		Fast mode		89		
t_{LOW}	LOW period of SCL clock	Standard mode		4.8		µs
		Fast mode		1.1		
t_{HIGH}	HIGH period of SCL clock	Standard mode		5		µs
		Fast mode		1.2		
$t_{VD:DAT}$	Data valid time	Standard mode		332		ns
		Fast mode		352		
$t_{HD:DAT}$	Data hold time	Standard mode		207		ns
		Fast mode		226		
$t_{SU:DAT}$	Data set-up time	Standard mode		4.8		µs
		Fast mode		1.0		

Note,
1. IO Driver configuration 0 (week driver capability)

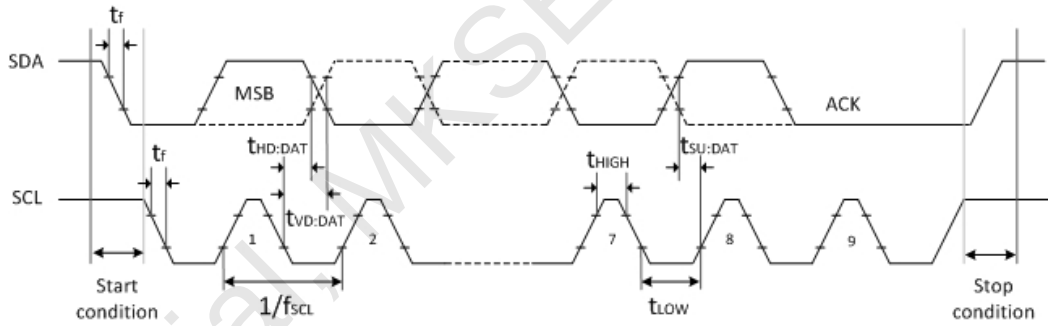


Figure 11 I2C-bus clock timing

MK8000 series support 7-bit address formats and 10-bit address formats,

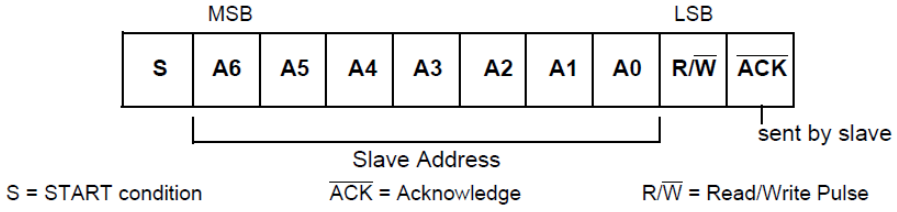


Figure 12 *7-bit address formats*

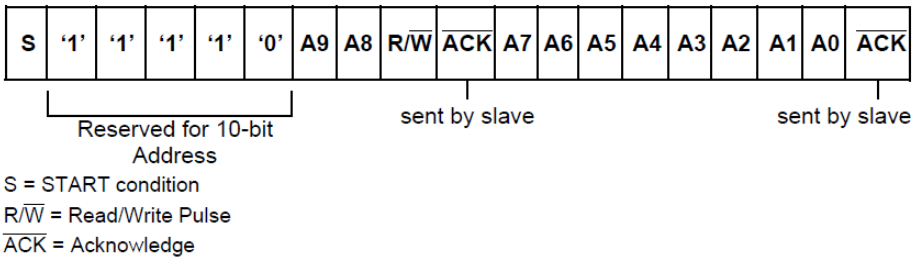


Figure 13 *10-bit address formats*

5.6.5 UART Parameters

Table 26 Baud Rate Supported

(Typical values are T_A = 25°C and VCC=3V).

Baud Rate	Conditions	Error Rate
1,200	Sysclk = 62.4MHz	0.00%
2,400		0.00%
4,800		0.00%
9,600		0.00%
14,400		0.00%
19,200		0.00%
28,800		0.00%
31,250		0.00%
38,400		0.00%
57,600		0.03%
115,200		0.25%
230,400		0.31%
460,800		0.31%
921,600		0.43%
1,000,000		0.65%
2,000,000		2.50%

6. Reference design

6.1 Schematic design

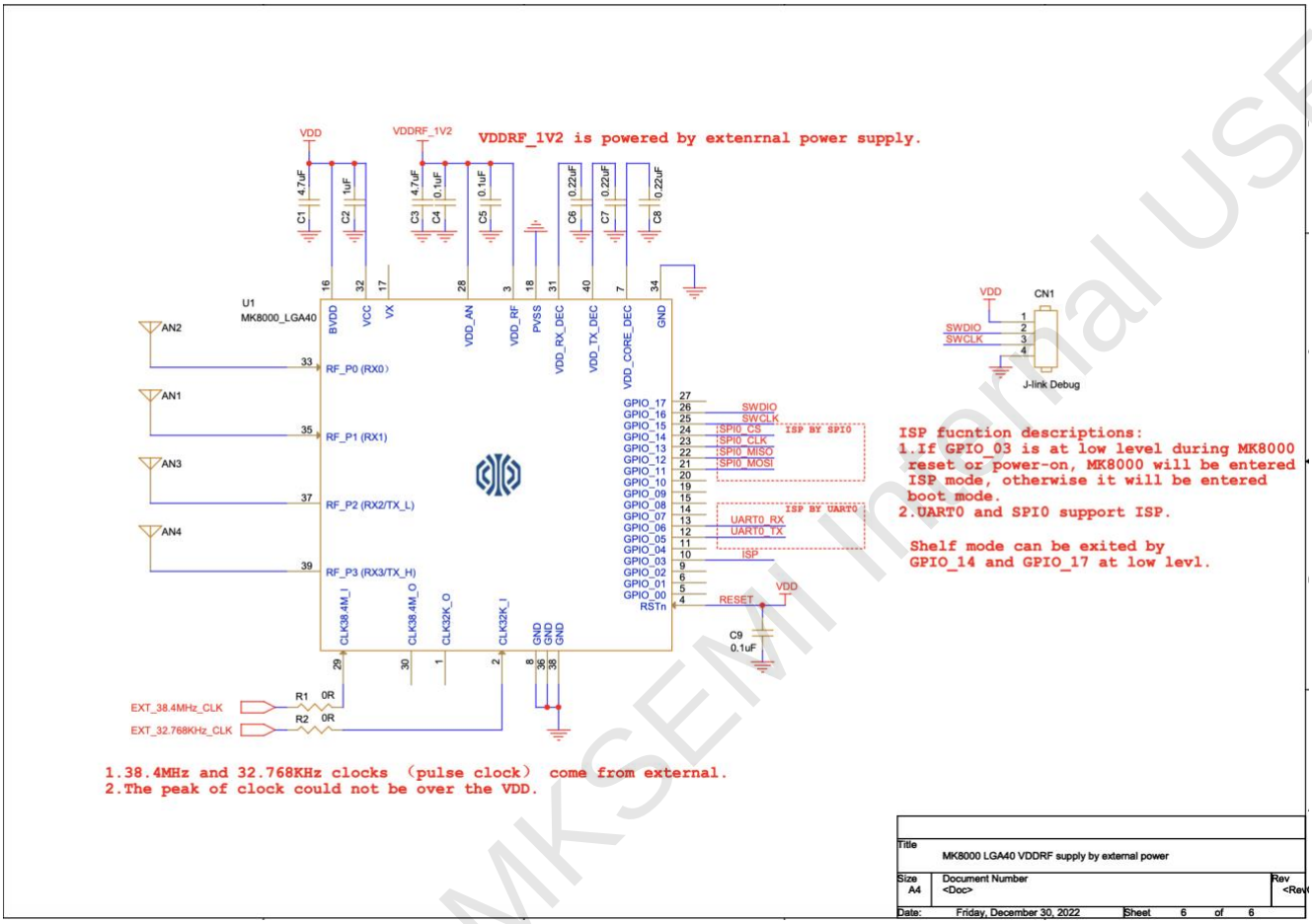


Figure 14 Reference design without DCDC

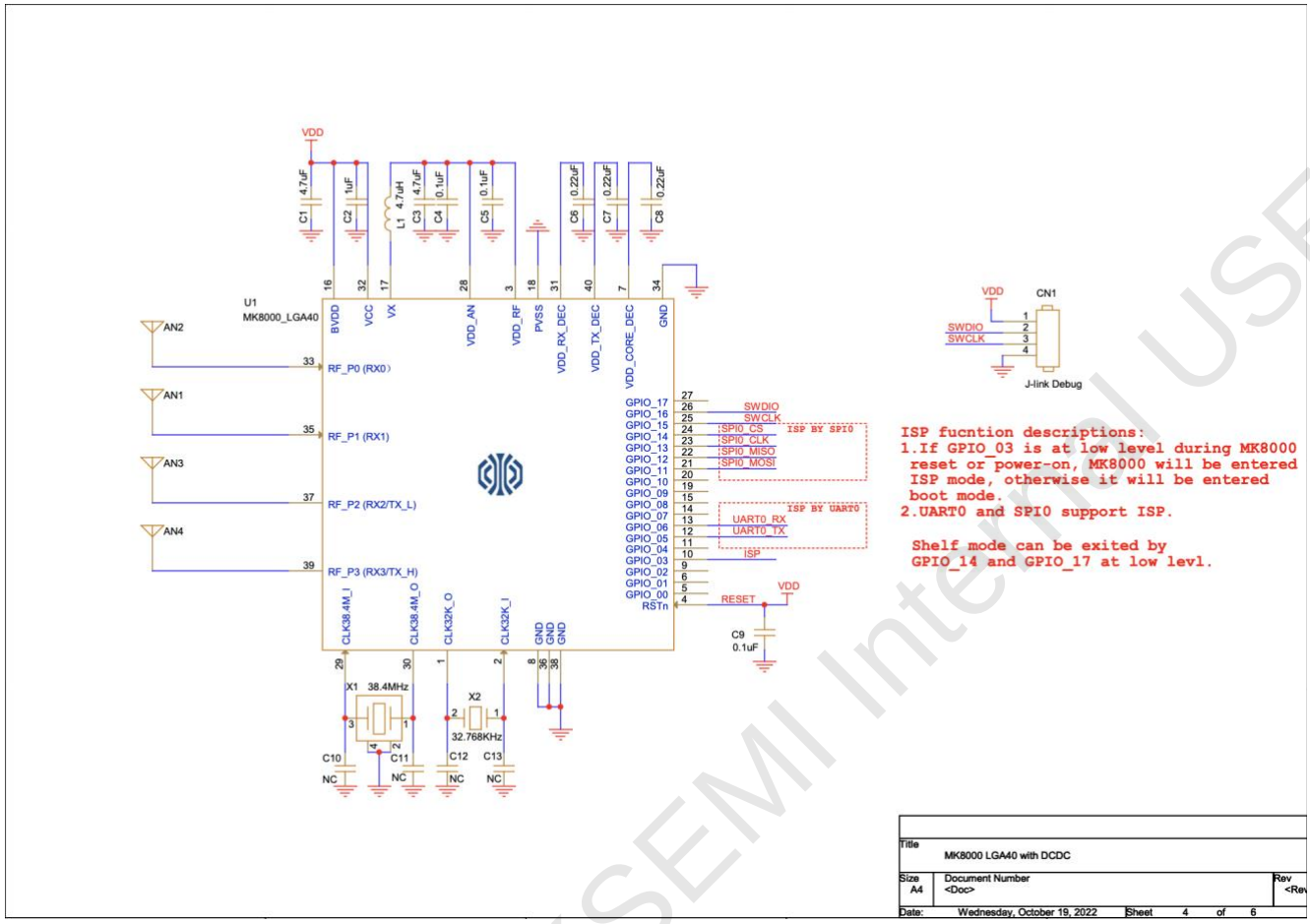
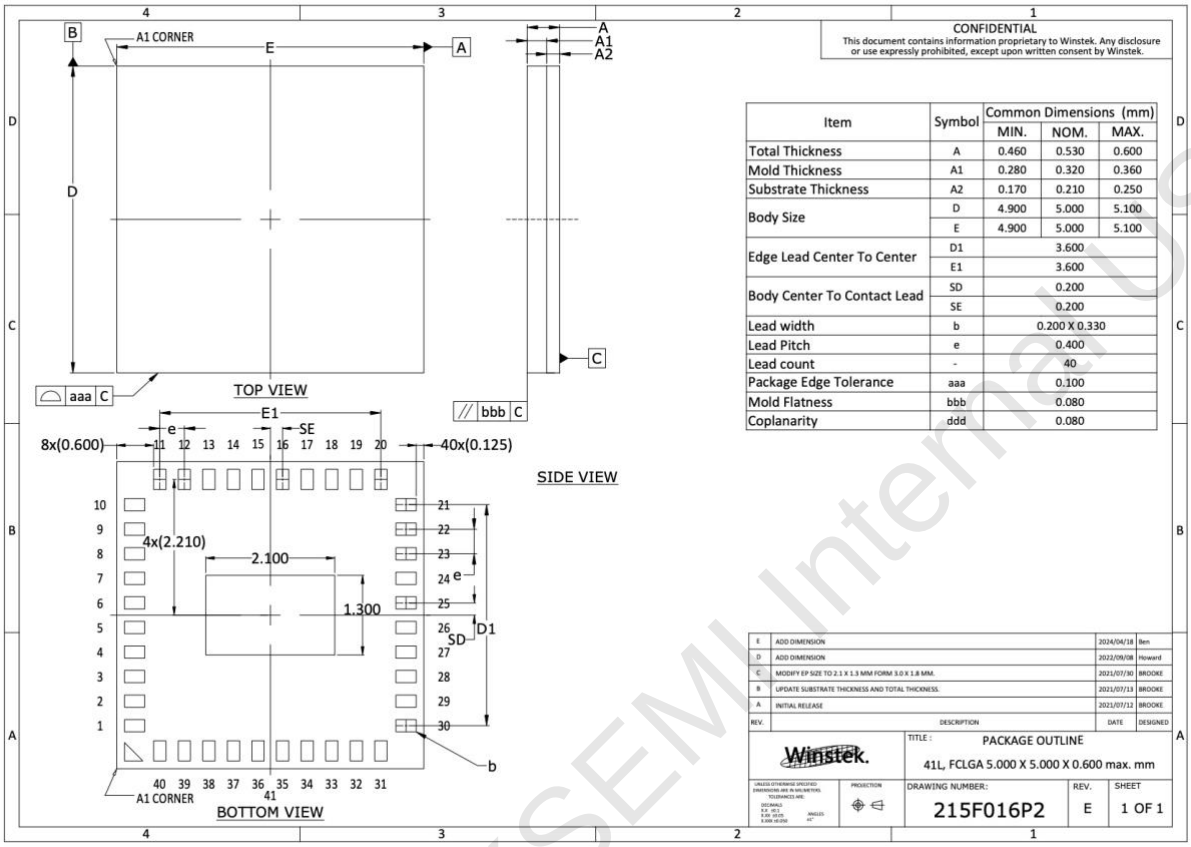


Figure 15 Reference Design with DC/DC and Crystal

7. Package information



Item	Symbol	Common Dimensions (mm)		
		MIN.	NOM.	MAX.
Total Thickness	A	0.460	0.530	0.600
Mold Thickness	A1	0.280	0.320	0.360
Substrate Thickness	A2	0.170	0.210	0.250
Body Size	D	4.900	5.000	5.100
	E	4.900	5.000	5.100
Edge Lead Center To Center	D1		3.600	
	E1		3.600	
Body Center To Contact Lead	SD		0.200	
	SE		0.200	
Lead width	b		0.200 X 0.330	
Lead Pitch	e		0.400	
Lead count	-		40	
Package Edge Tolerance	aaa		0.100	
Mold Flatness	bbb		0.080	
Coplanarity	ddd		0.080	

REV.	DESCRIPTION	DATE	DESIGNED
E	ADD DIMENSION	2024/04/18	Ben
D	ADD DIMENSION	2022/09/08	Howard
C	MODIFY EP SIZE TO 2.1 X 1.3 MM FORM 3.0 X 1.8 MM.	2021/07/30	BROOKE
B	UPDATE SUBSTRATE THICKNESS AND TOTAL THICKNESS.	2021/07/13	BROOKE
A	INITIAL RELEASE	2021/07/12	BROOKE

Figure 16 LGA40

8. Ordering information

Table 27 MK8000xxx Ordering Information

IC name, which is same as the mask in IC package. In this name, it contains MCU type/BLE/USB or UWB	Chip Version: A~Z	P: Package type, C, CSP Q, QFN B, BGA L, LGA …;	Pin number, 08 – 8 pins 0A – 16 pins 20 – 32 pins 28 – 40 pins 30 – 48 pins 31 – 49 pins 64 – 100 pins …	Memory Size: (Flash) N – No Flash D – 256K E – 512K F – 1M, … Other letters can be used for special memory size	Temperature Range, G: -40 ~ 85 I: -40 ~85 A: -40 ~ 105 …	Flash Vender, V, For None M, MXiC G, GD P, Puran/Puya Z, Zbit …

9. Append

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